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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/594,510	06/16/2000	Alan G. Wood	M4065.0184/P184	2407

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/594,510	WOOD ET AL.	
	Examiner	Art Unit	
	Chuong A Luu	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 35-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 35-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (U.S. 6,153,448) in view of Smith (US 6,064,217).

Takahashi discloses a method of forming a semiconductor device with

(1); (11) forming a layered assembly by attaching a substrate "wafer" (1) to an insulating layer (12) "dielectric layer" (see Figure 2);

forming conductive structures (13) in contact with a top surface of said insulating layer (12) "dielectric layer" (see Figure 2);

forming input/output devices (14) in contact with said conductive structures (13);

subsequently, dicing said layered assembly (see column 3, lines 28-32. Figure 4C);

(2) further comprising the step of connecting said semiconductor devices to input/output devices on the dielectric layer (see Figure 2);

(5) wherein said step of forming said layered assembly includes the step of adhering said wafer to said insulating layer (12) "dielectric layer" (see Figure 2);

(6) further comprising the step of electrically connecting said semiconductor devices to ball grid arrays (14) on said insulating layer (12) "dielectric layer" (see column 7, lines 51-55. Figures 2 and 4C);

(8) wherein said connecting step comprises the step of connecting solder bumps (14) on said wafer to circuit traces on said insulating layer (12) "dielectric layer" (see Figures 2 and 4C);

(9); (17) wherein said dicing step is performed by a saw (see column 8, line 63);

(10) further comprising the step of providing an electrode pad (15) in said layered assembly (see Figures 2 and 4C);

(12) wherein said forming step comprises the step of adhering said substrate (1) "wafer" to said electrode pad (15) (see Figure 2 and 4C);

(7); (13); (14) wherein said connecting step comprises the step of locating wire patterns (13) "bonds" in openings through said insulating layer (12) "dielectric layer" (see Figures 2 and 4C);

(15) wherein said connecting step comprises the step of connecting solder bumps (14) on said substrate (1) "wafer" to conductive traces (13) on said insulating layer (12) "dielectric layer" (see Figure 2);

(16) further comprising the step of connecting said traces to conductive vias extending through said insulating layer (12) "dielectric layer" (see Figure 2).

Takahashi teaches everything above except for describing testing semiconductor devices in said wafer. However, Smith discloses a reusable test socket with **(1); (11)...** subsequently, testing semiconductor devices in said wafer (see column 4, lines 27-45); **(3)** wherein said testing is conducted through said input/output devices (see column 9, lines 3-20); **(4)** further comprising the step of discarding one or more defective packages (see column 12, lines 2-13); **(18)** further comprising the step of testing said

semiconductor devices through said ball grid arrays (see column 4, lines 27-45). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings above to conduct testing to determine whether the chips are good or bad before further completion the fabrication a semiconductor device.

Claim 19 is rejected under 35 U.S.C. 102(e) as anticipated by Lam (U.S. 6,344,401 B1).

Lam discloses a method of forming a stacked-die integrated circuit chip package on a wafer level with

(19) aligning a semiconductor wafer with respect to an adhesive layer (18) "dielectric tape" (see Figures 5-6);

subsequently, connecting semiconductor devices in said wafer (21) to ball grid arrays (50) on said adhesive layer (18) "dielectric tape" (see Figures 6-7);

simultaneously, dicing said wafer and said adhesive layer (18) "dielectric tape" (see column 4, lines 1-57. Figures 6-8).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lam (U.S. 6,344,401 B1) in view of Gaynes et al. (U.S. 6,165,885)

Lam teaches the above outlined features except for optically aligned. However, Gaynes discloses a method of making components with solder balls by **(20)** wherein said wafer is optically aligned with respect to said dielectric tape (see column 16, lines

18-29). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings above by optically aligned semiconductor components to manufacture integrated circuit devices.

Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lam (U.S. 6,344,401 B1) in view of Gaynes et al. (U.S. 6,165,885), and further view of Huddleston et al. (U.S. 5,834,320)

Lam and Gaynes teach everything above except for magnetically aligned with a magnet ring. Furthermore, Huddleston discloses a method of assembling a semiconductor device using a magnet (see columns 7 and 8, lines 44-67 and lines 1-51, respectively). It would have been obvious to one having ordinary skill in the art at the time the invention was made to magnetically aligned with a magnet ring to form a semiconductor device.

Claims 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lam (U.S. 6,344,401 B1) in view of Kobayashi et al. (U.S. 4,781,969)

Lam discloses a method of forming a stacked-die integrated circuit chip package on a wafer level with

(35) connecting said semiconductor devices to respective ball grid arrays (50) located on said substrate (see Figures 6-8);

testing said semiconductor devices through said ball grid arrays (see column 4, lines 16-34);

(37) further comprising the step of singulating packages from said wafer and said substrate (see column 4, lines 1-57).

Lam teaches everything above except for using a flexible substrateg packages. However, Kobayashi discloses a printed circuit board with **(35).....** adhering said wafer to a flexible substrate (see column 1, lines 38-43). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Lam and Kobayashi by using a flexible substrate for fabricating a semiconductor device to exceed its performance criteria.

Claims 36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lam (U.S. 6,344,401 B1) in view of Kobayashi et al. (U.S. 4,781,969), and further view of Lam (5,137,836)

Lam and Kobayashi diclose everything above except for identifying defective packages. Furthermore, Lam (836) discloses a method of manufacturing a repairable multi-chip module by **(36);** **(38)** further comprising the step of segregating defective packages from other packages (see column 3, lines 1-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings above to identifying one or more defective chip during fabrication of a semiconductor device.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and (703)872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

CAL
July 15, 2002

VUTHE SIEK
PRIMARY EXAMINER